A Study on a Multi-Disciplinary Optimization Method for the PMP

Soon-Young Seo*, Jae-Woo Jeong, Dong-Hyeob Cho, Hyuk Kim
Micro Nano Technology Research Team, Mechatronics & Manufacturing Technology Center, Corporate Technology Operations, Samsung Electronics Co. Ltd.

Abstract

In the mobile electronic appliances market, the feature of products is getting smaller, thinner and more multi-functional. Therefore, mobile products are easily damaged from drop/impact and thermal cycling load. To make them more reliable under these conditions, the junction area between chips and PCB should be designed to bear up under drop/impact. And the heat caused by main chip (Memory & DMB channel chip) should be dissipated as quickly as possible. From the viewpoint of CAE simulation, although those two problems (drop & heat) should be considered simultaneously, they should not. Because the outline of PCB mainly depends on the location of main chip, positioning the main chip is one of the most important steps in the initial design stage. And the dynamic stress from free drop and heat caused by main chip are the one of the most critical factors to position the main chip. This paper presents the design process for positioning the main chip on PCB of PMP using MDO method. That is, the trade-off design variables between drop and thermal loading analysis were identified and system level optimization is performed in parallel.
The main theme of this paper is to provide a way to get MDO solution of the PMP model in the early design stage.

Introduction

Generally, most of designers depend on their experience in designing the mobile electronic products. Especially, when they design the PCB (Printed Circuit Board), it is difficult to find the adequate location of main chip (Memory & DMB channel chip in PMP) and accessories on PCB. Usually, they rely on the several useful tips. For example, avoid positioning it on the mount point and arrange the chip considering the deformation of the PCB…etc. So the purpose of this paper is to propose the guideline of PCB design to designers.

Most of mobile products in market show serious problem in the area of drop and thermal cyclic loading. First, structural problems happen in the drop/impact test. The serious phenomenon occurred at the outermost solder bumps that join the chip and PCB. The crack on solder bump propagates along the interface between bump and PCB pad. To improve the drop impact reliability, equivalent plastic strain solder bumps should be minimized. Second, thermal problems result from heat caused by the main chip therefore the heat should be dissipated as quickly as possible. Even though those two problems should be solved simultaneously, they should not usually. After all, some kinds of common design variables, which affect the location of chips, are defined and then the equivalent plastic strain and temperature would be optimized with linear combination of each regression formula which obtained using RSM in this study.

Wong et al. [1-2] established the mechanics and physics of failure in a typical board-level test and identified a weakness in the drop impact strength of SnAgCu solder alloy. Lim et al. [3] surveyed the impact behavior of several mobile phones and personal digital assistants (PDAs) at various impact orientations. Zhu [4] applied modeling technique to assess reliability performance of a portable electronic product, mobile phone subjected to drop impact loads. Tee et al. [5] proposed a life prediction model for board level drop test to estimate the number of drops to

failure for a package, and studied on various testing parameters of TFBGA (Thin-profile Fine-pitch BGA) and VFBGA (Very-thin profile Fine-pitch BGA) packages.

Method of Analysis

Method of analysis is divided into 4 parts. At the 1st stage, the original FE Model was correlated with test result within 5% range of error to make it reliable. Second, drop/impact simulation with correlated FE Model was performed with 5 faces (front, left, right, top, bottom), in order to decide which direction the model would be dropped. The purpose of drop/impact simulation is to decide the location of main chips minimizing the equivalent plastic strain on the solder bump modeled as beam element. Third, thermal analysis was performed by ANSYS in main chips on PCB. The aim of thermal analysis is to find out the temperature distribution of PCB which emitted by main chips. At the final stage, the MDO was performed to find out the optimal position of main chips considering the drop and thermal effect simultaneously.

Drop/Impact Test and Correlation

Drop/impact test was performed by Lansmont shock system just like Figure 1. The PMP was fixed on the steel block by steel bar. And two accelerators were used. One is fixed on the steel block and it is to be used for reference input acceleration. The other was fixed on the center of PMP just like Figure 1. As doing this, we know the acceleration of PMP relative to the reference acceleration. (In this test reference acceleration set to 1400G, where 1G is the 9.8 m/s^2). Figure 2 (a) shows the test result of acceleration. In that case, the peak value of acceleration on the PMP is the 1940G. This condition of test is applied to the simulation in the same way. And Figure 2 (b) shows the simulation result. In that case of simulation the peak value of acceleration in PMP is 2015G. Percent variation of test and simulation is about 4%. That means the FE Model was well correlated to test result.

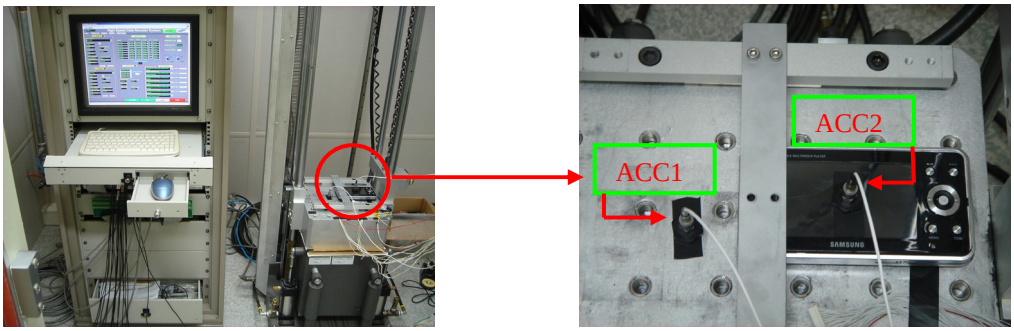
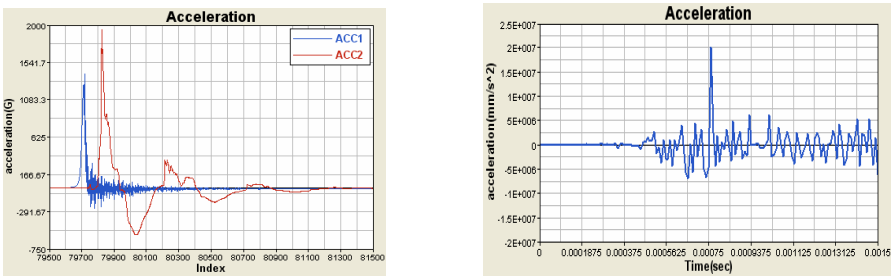


Figure 1. Experimental Set Up



(a) Test result **(b) Simulation result**

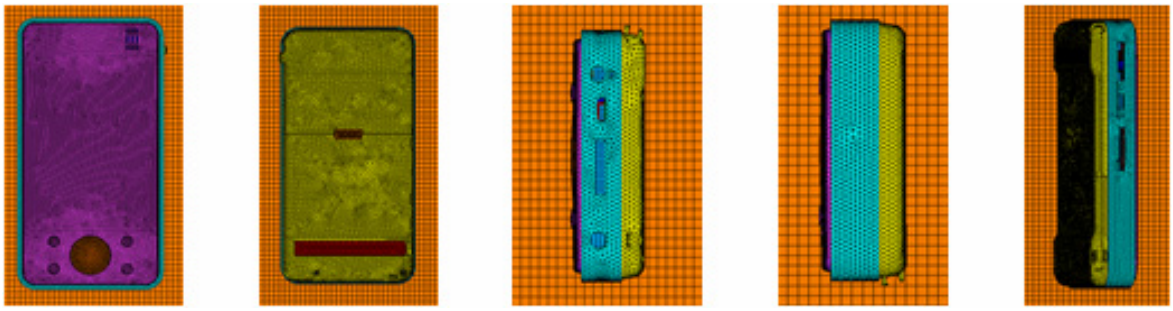
Figure 2. Acceleration graph : (a) Test result, (b) Simulation result

Drop/Impact Simulation

Total numbers of elements are 254,076 and nodes are 138,595. Total weight of product is 350g, and mass density of components was tuned to adjust the total weight in simulation. Velocity just before product hit the ground was imposed on the model as a initial velocity as below.

Initial velocity $v = \sqrt{2gh} = \sqrt{2*9800*800} = 3960 mm/s$

Figure 3 shows the direction of surface in drop/impact simulation.



(a) Bottom (b) Top (c) Left (d) Right (e) Front

Figure 3. Drop/impact simulation in 5 drop surfaces

Thermal Analysis

Many components except for 3 main chips, which generate high temperature heat, were modeled as simply as possible. The thermal properties were tuned and the heat conduction analysis was performed. Figure 4 shows the initial position of three main chips on front/back surface of PCB.

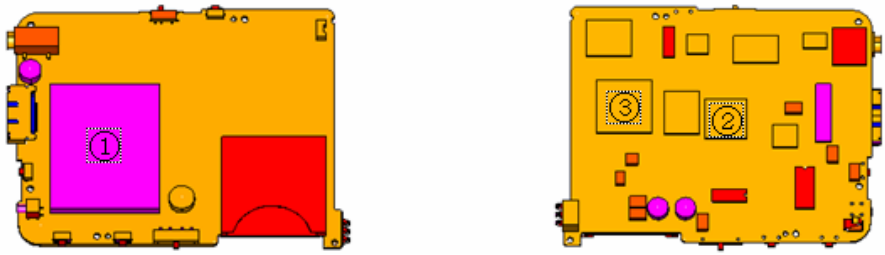


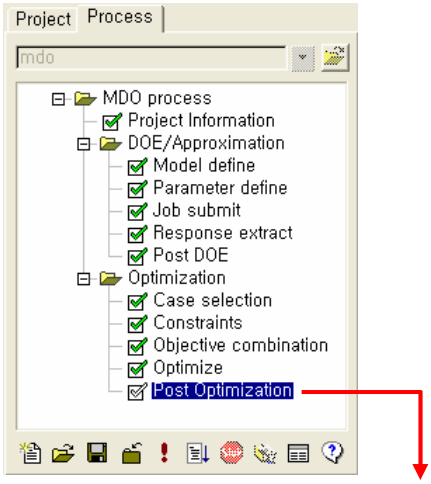
Figure 4. Position of main chips

- Chip 1 : DMB channel chip and tuner
  (Quantity of emitted heat : 720mW, measured emitted temperature : 52.1℃)
- Chip 2 : S3CA470
  (Quantity of emitted heat : 100mW, measured emitted temperature : 58.2℃)
- Chip 3 : DA320
  (Quantity of emitted heat : 726mW, measured emitted temperature : 59.7℃)

MDO Process

MDO process was set up using many kinds of computer language and program as shown in Figure 5. There are two modules in that process. First one is DOE/Approximation module. In that module, analysis type, design parameter and others are defined and submit a job to super computer to get responses and RSM (Response Surface Method) approximation. The other is optimization, which define constraints and objective function of MDO (multi object function which has linear combination) and then perform the optimization to find the trade off value.

Anyone who knows the optimal design theory can use this process easily. In this paper, MDO process was performed after selecting the common variables in the drop/impact and thermal analysis.



Post Processing Optimization

#	Objective	Improvement(%)	Max_plastic_strain	chip1_y	chip2_x	chip2_y	chip3_x	chip3_y	chip1_y	chip2_x	chip2_y	chip3_x	chip3_y
1	985.908	100.0	0.0322101	0	0	0	0	0	0	0	0	0	0
2	986.274	100.037123139	0.0340171	1.0428	0	0	0	0	1.0428	0	0	0	0
3	984.401	99.8471459812	0.0331634	0	1.0428	0	0	0	0	1.0428	0	0	0
4	983.877	99.7939970058	0.0247127	0	0	1.0428	0	0	0	0	1.0428	0	0
5	979.614	99.3616037196	0.0325335	0	0	0	1.0428	0	0	0	0	1.0428	0
6	980.771	99.4789574686	0.0307106	0	0	0	0	1.0428	0	0	0	0	1.0428
7	984.354	99.8423788021	0.0315017	-0.105	0.11	0.09	0.095	0.1	-0.105	0.11	0.09	0.095	0.1
8	977.461	99.1432263457	0.0318053	-0.11	0.09	0.095	1.25136	0.105	-0.11	0.09	0.095	1.25136	0.105
9	975.047	98.8983759134	0.0312161	-0.02	0.185	0.195	1.51415	0.215	-0.02	0.185	0.195	1.51415	0.215
10	972.803	98.6707684693	0.0318849	-0.115	0.285	0.09	1.84726	0.305	-0.115	0.285	0.09	1.84726	0.305
11	970.164	98.403096435	0.031126	-0.215	0.39	0.2	2.17976	0.4	-0.215	0.39	0.2	2.17976	0.4
12	968.335	98.2175821679	0.030461	-0.32	0.5	0.29	2.37	0.5	-0.32	0.5	0.29	2.37	0.5
13	967.5	98.1328886671	0.0296883	-0.43	0.59	0.385	2.37	0.605	-0.43	0.59	0.385	2.37	0.605
14	966.525	98.0339950584	0.0288728	-0.49286	0.7021	0.485	2.37	0.7381	-0.49286	0.7021	0.485	2.37	0.7381

Apply
Prev
Next

Figure 5. MDO process

Simulation Result

As shown in Figure 6 and Table 1, the highest equivalent plastic strain on solder bump was obtained in case of top surface drop. Therefore the optimization work would be conducted in that case. Figure 7 shows the thermal distribution of whole product and DA320 chip which is a kind of main chip

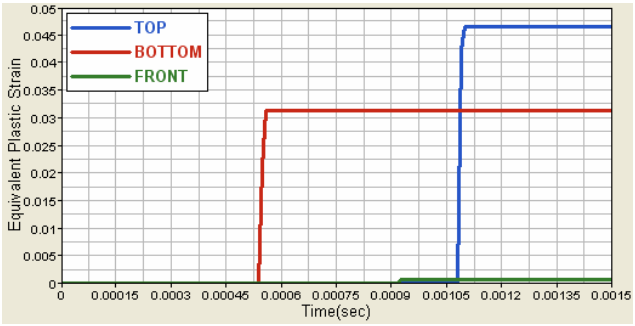
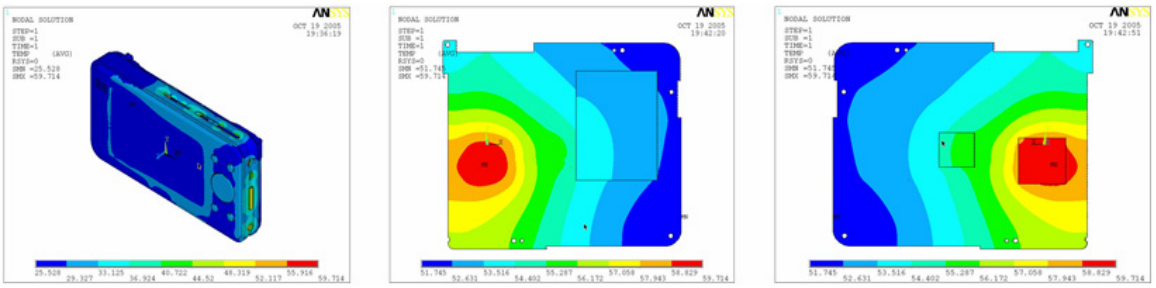


Figure 6. Equivalent Plastic Strain curves

Table 1. Equivalent Plastic Strain in 5 surfaces drop

	Top	Bottom	Front	Right	Left
Equivalent Plastic Strain	4.7%	3.1%	0.06%	0%	0%



(a) Product (b) DA320 chip in front PCB (c) DA320 chip in back PCB

Figure 7. Temperature range : (a) Whole product, (b) DA320 chip in front PCB, (c) DA320 chip in back PCB

Improved Design

Through the MDO method, final solution of optimal position of main chips is like as shown in Figure 9. Figure 8 shows just movable range of main chips considering structure layout. Figure 10, Figure 11 and Table 2 shows the plot of equivalent plastic strain of solder ball and temperature of PCB and rate of improvement. With optimum variables, the equivalent plastic strain decreased to 38.3% and temperature decreased to 4.0% compared to initial design. Even if the improvement of temperature is not so big absolutely, if should be taken into account because that amount of improvement is kind of large considering the range of possibility. Figure 12 (a) shows the variables which are critical to plastic strain. In this plot, we know the change of y coordinate of chip2 is the most influential factor to plastic strain. Figure 12 (b) shows the variables which are critical to temperature. We find that the change of x, y coordinate of chip3 influence on the temperature. Figure 13 shows the characteristic of response according to the change of design parameter level (-2.37, -1, 0, +1, +2.37). Figure 14 shows the regression formula was obtained by Response Surface Method. As shown in Figure 12, the most influential factors are y coordinate of chip2, x, y coordinate of chip3. Therefore the regression equation for those variables should be obtained. And the equivalent plastic strain and temperature of main chips decrease monotonically with increasing y coordinate of chip2, and x, y coordinate of chip3.

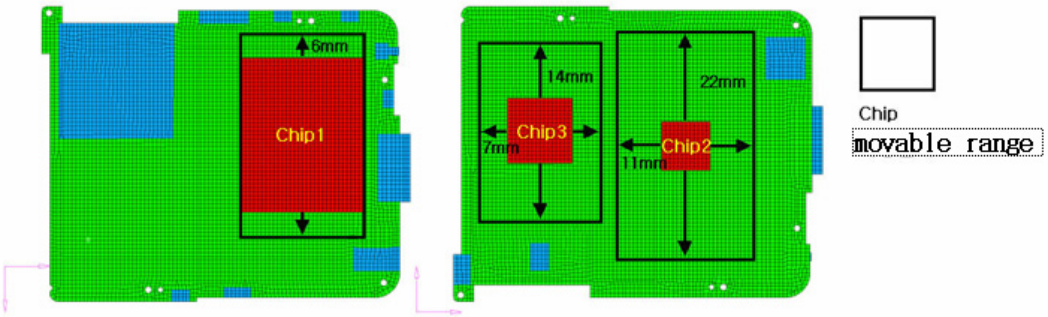


Figure 8. Equivalent Plastic Strain curves

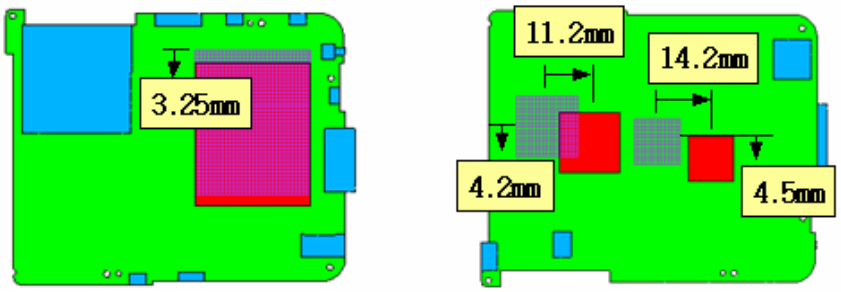
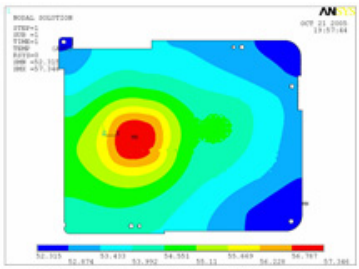
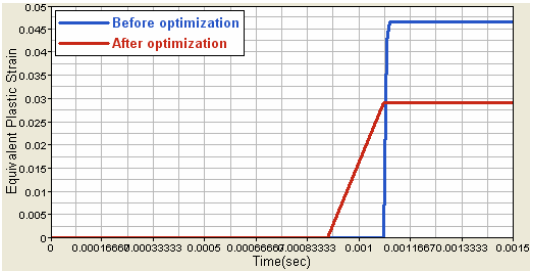


Figure 9. Optimal position of chips in front, back PCB



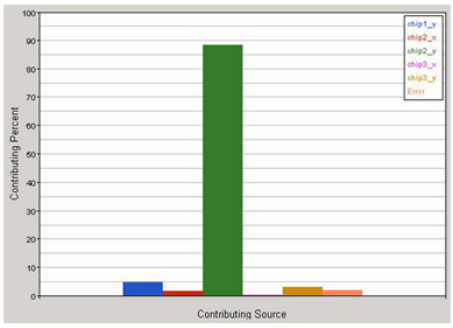


(Left) Figure 10. Temperature range after improved design

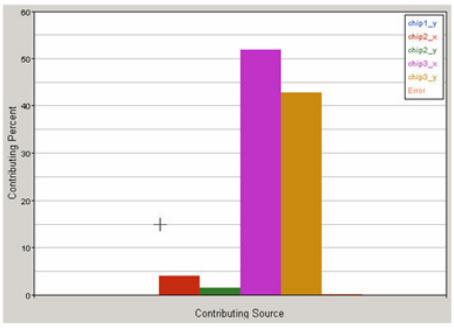
(Right) Figure 11. Equivalent plastic strain before/after optimization

Table 2. Compare before/after optimization in strain and temperature

	Before improvement	After improvement	% variation
Equivalent plastic strain	0.047	0.029	38.3
Temperature(℃)	59.7	57.3	4.0

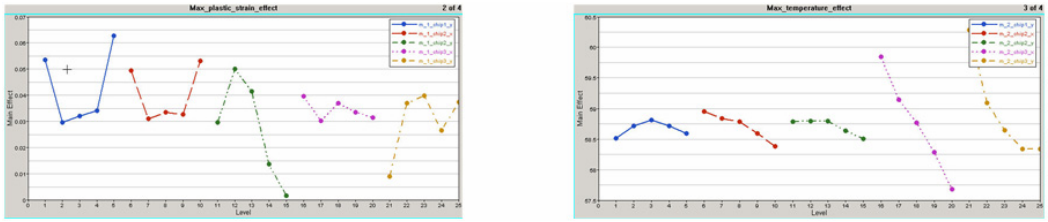


(a) Equivalent plastic strain



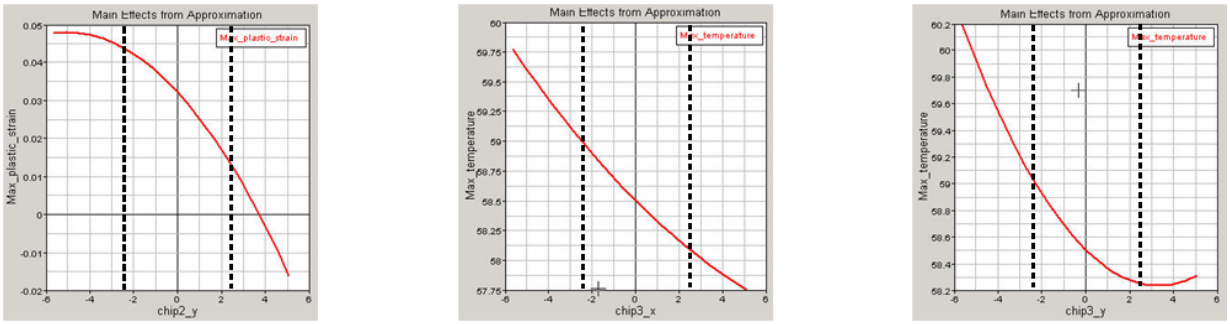
(b) Temperature

Figure 12. Pareto chart : (a) Equivalent plastic strain, (b) Temperature



(a) Equivalent plastic strain (b) Temperature

Figure 13. Main effect : (a) Equivalent plastic strain, (b) Temperature



(Left) (a) Plastic strain fluctuation curve according to the y coordinate change of chip2
(Center) (b) Temperature fluctuation curve according to the x coordinate change of chip3
(Right) (c) Temperature fluctuation curve according to the y coordinate change of chip3

Figure 14. Regression formula by RSM

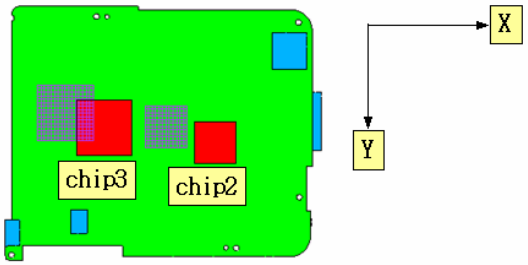


Figure 15. The coordinate of chip2 and chip3

Conclusion

This paper provides a way how to get an optimal position of main chips in PCB of PMP by MDO method. Currently, just only the structural and thermal effects are considered in Samsung MDO process. So further research on electro-magnetic fields of mobile product is required to be done and the module for that field should be added to the MDO process. And then MDO method helps the release engineer design the PCB in the concept design stage and eventually save the cost in the reliable test and reduce the period of mass product.

References

[1] E.H. Wong, K.M. Lim, N.T.S. Lee, S.K.W. Seah, C. Hoe, J. Wang, "Drop Impact Test - Mechanics & Physics of Failure," Proc 4th EPTC, pp. 327-333, 2002

[2] E.H. Wong, C.T. Lim, J.E. Field, V.B.C. Tan, V.P.W. Shim, K.M. Lim, S.K.W. Seah, "Tackling the drop impact reliability of electronic packaging," IPACK 2003.

[3] C.T. Lim, C.W. Ang, L.B. Tan, S.K.W. Seah, E.H. Wong, "Drop Impact Survey of Portable Electronic Products," Proc 2003 ECTC, pp. 113-120.

[4] Liping Zhu, "Modeling Technique for Reliability Assessment of Portable Electronic Product Subjected to Drop Impact Loads," Proc 2003 ECTC, pp. 100-104.

[5] T.Y. Tee, H.S. Ng, C.T. Lim, E. Pek, Z. Zhong, "Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications," Proc 2003 ECTC, pp. 121-129.